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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,515	08/27/2003	Masataka Kusumi	60188-631	3985

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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,515	KUSUMI ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1 and 2 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Newly amended claim 1 includes the limitation of "*a third insulating film* interposed between the floating gate and the semiconductor substrate", however dependent claim 2 also discloses "a *third insulating film* formed on each of the control gate electrodes." Thus, the claims are structurally unclear since both disclose a "third insulating film" on different portions of the claimed invention.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 8 and 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art as disclosed in figures 10A-19, and their description on pages 2-8 of the instant application, in view of Yamauchi (U.S. Patent No, 5,338,952) and further in view of Yuan et al. (U.S. Patent No. 6,512,263). With regard to Claim 1, Applicant's admitted prior art discloses a semiconductor memory device (page 2, lines 4-5) comprising:

a plurality of isolations (202) formed on a semiconductor substrate (201);

a plurality of active regions defined on the semiconductor substrate and isolated from each other by the isolations (figure 15C);

a plurality of control gate electrodes (204) formed over the semiconductor substrate, each said control gate electrode crossing all of the isolations and all of the active regions (figure 15A) with a first insulating film (203) interposed between the control gate electrode and the semiconductor substrate (figure 15B); and

a plurality of floating gate electrodes (210C), each of which is formed for associated one of the active regions so as to cover a side-face of associated one of the control gate electrodes with a second insulating film (209) interposed between the floating gate electrode and the control gate electrode and also interposed between the floating gate (210C) and the substrate (201) (figures 15B and 16B),

wherein the isolations are spaced apart from each other along the width of the control gate electrodes (figure 15A) and

wherein each of said isolation crosses all of the control gate electrodes (figure 15A).

Applicant's admitted prior art fails to disclose the claimed third insulating film interposed between the floating gate and the substrate, wherein the second insulating film includes material different from that of the third film, and it also fails to disclose the claimed isolations extend continuously along the length of the control gate electrodes. However, Yamauchi discloses on figure 1 a non-volatile memory device, which includes a substrate (1), an auxiliary gate (4), a floating gate (11a), an insulating layer (30) between the auxiliary gate (4) and the floating gate

(11a) and another insulating layer (9) between the floating gate (11a) and the substrate (1), wherein insulating layer (9) comprises a material different from that of insulating layer (30) (column 3, lines 49-52 and column 4, lines 12-15). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed the claimed third insulating film interposed between the floating gate and the substrate, wherein the second insulating film includes material different from that of the third film, as suggested by Yamauchi, in order to provide an insulating layer between the floating gate and the substrate for tunneling purposes (column 3, lines 49-52) and an insulating layer which may comprise a two-layer or three layer film including materials different from said insulating layer between the floating gate and the substrate, to further enhance insulation between the floating gate and an auxiliary gate (column 4, lines 12-15).

Regarding the claimed isolations extending continuously along the length of the control gate electrodes, Yuan discloses a non-volatile memory cell array, which includes steering gates (81-86), which act as control gates for the memory cell array, that are crossed by isolation trenches (72, 73, 74) extending continuously along their length (figures 2 and 3). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include isolations that extend continuously along the length of control gate electrodes, as suggested by Yuan, in order to provide a high-degree of electrical isolation between rows and cells (column 6, lines 14-16), as well as increase the data density of the memory device (column 6, lines 16- 28).

With regard to Claim 2, Applicant's admitted prior art discloses an insulating film (205) formed on each of the control gate electrodes (204), (figure 15B).

With regard to Claim 3, Applicant's admitted prior art discloses (figures 15B and 16B) active regions each having a plurality of step-regions (201a), each of which is overlapped by associated one of the floating gate electrodes (210C) and,

wherein in each of said active regions, source regions (215) are defined in respective upper parts of the step regions and a drain region (214) is defined below the step region (figure 17B).

With regard to Claim 8, Applicant's admitted prior art discloses a second insulating film (209) formed between an upper part of step region (201a) and the floating gate electrode (210C).

With regard to Claim 9, Applicant's admitted prior art fails to disclose the claimed stacked structure of a silicon dioxide film and a silicon nitride film for the second insulating film. However, Yamauchi discloses on figure 1 a non-volatile memory device, which includes an insulating layer (30) comprising a two-layer film of silicon oxide and silicon nitride (column 4, lines 12-14). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed stacked structure of a silicon dioxide film and a silicon nitride film for the second insulating film, as suggested by Yamauchi, in order to provide an insulating layer which

may comprise a two-layer or three layer film to further enhance insulation between the floating gate and an auxiliary gate (column 4, lines 12-15).

Response to Arguments

3. Applicant's arguments filed July 5, 2005 have been fully considered but they are moot in view of the new grounds of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
7/14/05

TOM THOMAS
SUPERVISORY PATENT EXAMINER